



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Yoshitaka UEDA  
Title: SEMICONDUCTOR DEVICE  
Appl. No.: 10/627,608  
Filing Date: 07/28/2003  
Examiner: N. W. Ha  
Art Unit: 2814

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR §1.56**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

**TIMING OF THE DISCLOSURE**

The listed documents are being submitted in compliance with 37 CFR §1.97(c), before the mailing date of either a final action under 37 CFR §1.113, a notice of allowance under 37 CFR §1.311, or an action that otherwise closes prosecution in the application.

**RELEVANCE OF EACH DOCUMENT**

As a statement of relevance, a translation of a portion of a Japanese Office Action that issued August 24, 2004 with respect to a counterpart Japanese patent application is provided below.

Claims 1-3, 7-10

References 1-3

Remarks

It is a known issue, as References 1-3 describe, that an NC terminal can be a cause of electrostatic discharge for the adjacent terminal. Short-circuiting for equipotential and grounding are known measures that are generally taken to prevent electrostatic discharge between two electrodes in semiconductor device field.

Claims 5-6, 12-17

References 1-3

Remarks

It is easy for a person skilled in the art to conceive employing general pattern formation technology of the semiconductor package manufacture as short-circuiting means.

Claims 4 and 11

References 1-3

Remarks

It is known in the art, as References 1-3 show, to employ electrostatic protective circuit.

Index of Cited References

1. JP 11-163247
2. JP 61-199651
3. JP 2002-198466

This Record of Prior Art Search Results does not constitute a reason for rejection.

Prior Art Literature

JP 2001-348305  
JP 01-238148  
JP 02-119171

An English translation of the foreign-language documents is not readily available. However, the absence of such translation does not relieve the PTO from its duty to consider the submitted foreign language documents (37 CFR §1.98 and MPEP §609). English language abstracts are attached.

Applicant respectfully requests that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

**STATEMENT**

The undersigned hereby states in accordance with 37 CFR §1.704(d) that each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in 37 CFR §1.56(c) more than thirty days prior to the filing of the information disclosure statement.

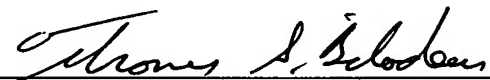
Applicant's statements regarding the Japanese Office Action are based on a partial translation that Applicant's representative obtained. These statements should in no way be considered as an agreement by Applicant with, or an admission of, what is asserted in the Japanese Office Action.


The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date: September 23, 2004

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Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

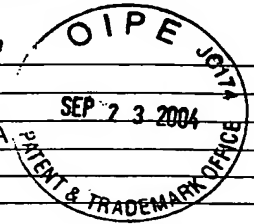
Date Submitted: September 23, 2004

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	10/627,608
Filing Date	07/28/2003
First Named Inventor	Yoshitaka UEDA
Group Art Unit	2814
Examiner Name	N. W. Ha
Attorney Docket Number	016891-0858


**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
	C1	JP	2002-198466		NEC IC MICROCOMPUTER SYSTEMS LTD.	07-12-2002		A
	C2	JP	2001-348305		TOSHIBA KK	12-26-2001		A
	C3	JP	11-163247		HITACHI LTD.	06-18-1999		A
	C4	JP	2-119171		HITACHI LTD.	05-07-1990		A
	C5	JP	1-238148		FUJI ELECTRIC CO. LTD.	09-22-1989		A
	C6	JP	1-199651		FUJITSU LTD.	09-04-1986		A

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>

Examiner Signature

Date Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

<sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.